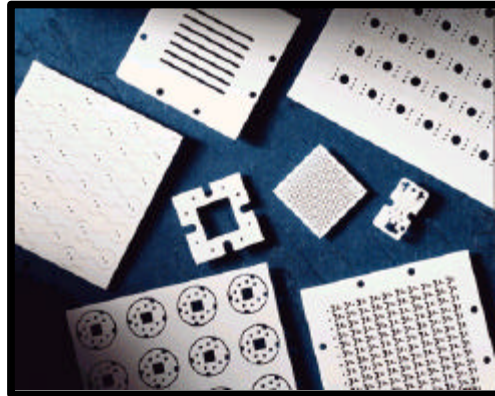


Ceramic Substrates for ICs



Introduction

The drive for increased microprocessor unit (MPU) performance has in turn expedited the development of higher on- and off- chip speeds, increased I/Os, greater I/O densities, higher power, and better power distribution. To satisfy these performance-driven needs, flip-chip packaging of high performance MPUs is becoming the standard. These faster ICs have led to a search for packages with lower resistance wiring and lower dielectric constant. In addition, the size of a typical high-performance MPU is 18 mm square or larger, making it important to find materials with a lower thermal coefficient of expansion (TCE) to match that of silicon. The higher numbers of on/off cycles and higher operating temperatures have made it clear that the controlled collapse chip connection (C4) process must allow for improved fatigue life. Furthermore the stress in the silicon itself grows proportionally to the TCE of the chip carrier as large die are attached and underfilled to the carrier. A number of ceramic substrates have been developed to meet these challenges (i.e. Glass Ceramic, 99.6% Aluminum oxide, 96% Aluminum oxide and Aluminum nitride) and are used in a variety of flip-chip multi-layer ceramic (MLC) packages (i.e. PGA, BGA, CGA, LGA).

The Measurement Need

High dimensional stability is critical for ceramic packages since the substrates must go through a heat treatment or "firing" in the packaging process. The pad locations before and after must be monitored to ensure that mating tolerances of upstream steps are being met.

